WHAT IS CLAIMED IS:

1. A data latch apparatus , comprising:

a first latch for latching a data signal;

a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative;

a restore device connected between said first and second latches and driven by a first power supply for transferring said data signal from said second latch to said first latch; and

said second latch powered by a second power supply other than said first power supply.

2. The apparatus of Claim 1, wherein said second latch includes a first node for providing said data signal to said restore device, said restore device including first and second transistors having respective gates connected to said first node.

3. The apparatus of Claim 2, wherein said first latch includes a plurality of transistors, each transistor of said plurality having a gate oxide, said first and second transistors having gate oxides that are thicker than said gate oxides of said plurality of transistors, said restore device including third and fourth transistors connected in series with said first and second transistors to form a series-connected transistor stack, said third and

fourth transistors having gate oxides which are thinner than said gate oxides of said first and second transistors.

4. The apparatus of Claim 3, wherein said first and second transistors are located at opposite ends of said transistor stack and are connected to said first power supply.

5. The apparatus of Claim 3, wherein said third and fourth transistors are connected at a common node other than said first node, and wherein said common node provides said data signal to said first latch.

6. The apparatus of Claim 1, wherein said second latch includes a node for providing said data signal to said restore device, said restore device including a transistor having a gate connected to said node.

7. The apparatus of Claim 1, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

8. The apparatus of Claim 1, wherein said second latch includes first and second nodes for providing said data signal to said restore device, said restore device including first

and second transistors having respective gates connected to said first and second nodes, respectively.

9. The apparatus of Claim 8, wherein said first latch includes a plurality of transistors, each transistor of said plurality having a gate oxide, said first and second transistors having gate oxides that are thicker than said gate oxides of said plurality of transistors, said restore device including third and fourth transistors connected in series with said first and second transistors, respectively, to form a differential pull-down network, said third and fourth transistors having gate oxides which are thinner than said gate oxides of said first and second transistors.

10. The apparatus of Claim 9, wherein said restore device includes a fifth transistor connected in series with said first and third transistors, and a sixth transistor connected in series with said second and fourth transistors, wherein said fifth transistor has a gate connected to said fourth transistor at a third node and said sixth transistor has a gate connected to said third transistor at a fourth node, and wherein said third and fourth nodes provide said data signal to said first latch.

11. A data processing apparatus, comprising:

data processing logic for performing data processing operations;

a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a plurality of data latch structures;

each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches and driven by a first power supply for transferring said data signal from said second latch to said first latch; and

said second latch powered by a second power supply other than said first power supply.

12. The apparatus of Claim 11, provided as one of a microprocessor, a microcontroller and a digital signal processor.

13. The apparatus of Claim 11, including a logic signal path connected to said restore devices for distributing said first power supply thereto.

14. A wireless communication apparatus, comprising:

an antenna structure for permitting communication via an air interface;

a digital data processor for performing digital data processing operations;

a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor;

said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a restore device connected between said first and second latches and driven by a first power supply for transferring said data signal from said second latch to said first latch; and

said second latch powered by a second power supply other than said first power supply.

15. The apparatus of Claim 14, provided as one of a mobile telephone, a laptop computer and a personal digital assistant.

16. A data latch apparatus , comprising:

a first latch for latching a data signal;

a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative;

a transfer device connected between said first and second latches for transferring said data signal between said first and second latches;

said first latch including a first plurality of transistors, each transistor of said first plurality having a gate oxide;

said second latch including a second plurality of transistors, each transistor of said second plurality having a gate oxide that is thicker than said gate oxides of said first plurality of transistors;

said transfer device including a transistor having a gate oxide that is thicker than said gate oxides of said first plurality of transistors; and

said first latch further for latching said data signal independently of contemporaneous operating characteristics respectively associated with said transistors of said second plurality and said transfer device.

17. The apparatus of Claim 16, wherein said transfer device includes a third plurality of transistors having respective gate oxides which are thicker than said gate oxides of said first plurality of transistors, said first latch further for latching said data signal independently of contemporaneous operating characteristics respectively associated with said transistors of said third plurality.

18. The apparatus of Claim 17, wherein said second latch includes a first node for providing said data signal to said transfer device, said third plurality of transistors including first and second transistors having respective gates connected to said first node.

19. The apparatus of Claim 18, wherein said transfer device includes third and fourth transistors respectively connected to said first and second transistors, said third and fourth transistors also connected together at a common node other than said first node.

20. The apparatus of Claim 19, wherein said common node provides said data signal to said first latch.

21. The apparatus of Claim 17, wherein said second latch includes first and second nodes for providing said data signal to said transfer device, said third plurality of transistors including first and second transistors having respective gates which are respectively connected to said first and second nodes.

22. The apparatus of Claim 21, wherein said transfer device includes third and fourth series-connected transistors connected in series with said first transistor, and fifth and sixth series-connected transistors connected in series with said second transistor, wherein said fourth transistor has a gate connected to said fifth transistor at a third node and said sixth transistor has a gate connected to said third transistor at a fourth node.

23. The apparatus of Claim 22, wherein said third and fourth nodes provide said data signal to said first latch.

24. The apparatus of Claim 16, wherein said second latch includes a first node for providing said data signal to said transfer device, said transistor of said transfer device having a gate connected to said first node.

25. The apparatus of Claim 16, wherein said operating characteristics are conductance characteristics.

26. The apparatus of Claim 16, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom.

27. A data processing apparatus, comprising:

data processing logic for performing data processing operations;

a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a plurality of data latch structures;

each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is

inoperative, and a transfer device connected between said first and second latches for transferring said data signal between said first and second latches;

said first latch including a first plurality of transistors, each transistor of said first plurality having a gate oxide;

said second latch including a second plurality of transistors, each transistor of said second plurality having a gate oxide that is thicker than said gate oxides of said first plurality of transistors;

said transfer device including a transistor having a gate oxide that is thicker than said gate oxides of said first plurality of transistors; and

said first latch further for latching said data signal independently of contemporaneous operating characteristics respectively associated with said transistors of said second plurality and said transfer device.

28. The apparatus of Claim 27, provided as one of a microprocessor, a microcontroller and a digital signal processor.

29. A wireless communication apparatus, comprising:

an antenna structure for permitting communication via an air interface;

a digital data processor for performing digital data processing operations;

a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor;

said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and a transfer device connected between said first and second latches for transferring said data signal between said first and second latches;

said first latch including a first plurality of transistors, each transistor of said first plurality having a gate oxide;

said second latch including a second plurality of transistors, each transistor of said second plurality having a gate oxide that is thicker than said gate oxides of said first plurality of transistors;

said transfer device including a transistor having a gate oxide that is thicker than said gate oxides of said first plurality of transistors; and

said first latch further for latching said data signal independently of contemporaneous operating characteristics respectively associated with said transistors of said second plurality and said transfer device.

30. The apparatus of Claim 29, provided as one of a mobile telephone, a laptop computer and a personal digital assistant.

31. A data latch apparatus, comprising:

a data signal input for receiving a data signal produced by a first logic device;

a latch coupled to said data signal input for retaining said data signal while the first logic device is inoperative; and

a driver coupled to said latch for, while the first logic device is inoperative, driving said data signal as retained in said latch to an input of a second logic device that remains operative while the first logic device is inoperative.

32. The apparatus of Claim 31, including an output coupled to said driver for providing said data signal to the input of the second logic device, and further including a further driver coupled to said data signal input and said output, said further driver for driving said data signal to the input of the second logic device while the first logic device is operative.

33. The apparatus of Claim 32, wherein said further driver includes an inverter having an input coupled to said data signal input and having an output, said latch coupled to one of said inverter input and said inverter output.

34. The apparatus of Claim 33, wherein said latch is coupled to both said inverter input and said inverter output.

35. The apparatus of Claim 32, including first and second transistors connected in parallel at first and second nodes, one of said nodes coupled to said further driver, and the other of said nodes for connection to a power supply used to power operation of the first logic device.

36. The apparatus of Claim 35, wherein said first and second transistors have respective gate oxides, and wherein said gate oxide of said first transistor is thinner than said gate oxide of said second transistor.

37. The apparatus of Claim 36, wherein said second transistor has a width-to-length ratio that is greater than a width-to-length ratio of said first transistor.

38. The apparatus of Claim 37, wherein said first and second transistors have respective gates that are connected together.

39. The apparatus of Claim 36, wherein said further buffer includes a plurality of transistors having respective gate oxides which are thinner than said gate oxide of said second transistor.

40. The apparatus of Claim 36, wherein said first and second transistors have respective gates that are connected together.

41. The apparatus of Claim 35, wherein said second transistor has a width-to-length ratio that is greater than a width-to-length ratio of said first transistor.

42. The apparatus of Claim 41, wherein said first and second transistors have respective gates that are connected together.

43. The apparatus of Claim 41, wherein said width-to-length ratio of said second transistor is at least about 30, and wherein said width-to-length ratio of said first transistor is at most about 10.

44. The apparatus of Claim 35, wherein said first and second transistors have respective gates that are connected together.

45. The apparatus of Claim 32, wherein said driver includes a plurality of transistors having respective gate oxides and said further driver includes a plurality of transistors having respective gate oxides, and wherein said gate oxides of said driver are thicker than said gate oxides of said further driver.

46. The apparatus of Claim 32, wherein said latch includes a plurality of transistors having respective gate oxides and said further driver includes a plurality of transistors having respective gate oxides, and wherein said gate oxides of said latch are thicker than said gate oxides of said further driver.

47. The apparatus of Claim 46, wherein said driver includes a plurality of transistors having respective gate oxides, and wherein said gate oxides of said driver are thicker than said gate oxides of said further driver.

48. The apparatus of Claim 31, wherein said driver is an inverter driver.

49. The apparatus of Claim 31, wherein said driver is for driving said data signal while the first logic device is inoperative due to removal of power therefrom.